REMARKS

The Office Action dated June 24, 2004 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

The specification has been amended to resolve an informality. Claims 1-8 also have been amended to more particularly point out and distinctly claim the subject matter of the invention. No new matter has been added. Applicants note that the amendments to the specification and claims were not made in response to a statutory rejection and that the claims are entitled to their full range of equivalents. Thus, claims 1-8 presently are pending in the application. Applicants respectfully submit claims 1-8 for consideration.

The specification was objected to because of an informality. The specification has been amended to resolve the informality. Thus, the objection is rendered moot.

Claims 1, 4, 6 and 7 were objected to because of informalities. Applicants have amended the claims to resolve the informalities. Thus, the objection is rendered moot.

Claims 6 and 7 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 6,032,271 (*Goodrum et al.*) The Office Action took the position that the cited reference taught each and every element of claims 6-7. Applicants respectfully submit that claims 6-7 are not disclosed or suggested by *Goodrum*.

Claim 6, upon which claim 7 is dependent, presently recites an interface circuit. The interface circuit includes means for connecting a first bus to a plug-in unit. The interface circuit also includes a first register. The interface circuit also includes a second

register. The interface circuit also includes means for transferring a bus address into the first register. The interface circuit also includes means for transferring the bus address, in conjunction with a reboot, from the first register into the second register.

As discussed in the specification, examples of the present invention enable a diagnostics program in a system to disconnect a defective plug-in unit from the system without requiring any actions on a user's part. Examples of the present invention locate faults in situations where bus release is not monitored in conjunction with the addressing sequence. Thus, the registers included in the interface circuit may be economically implemented, so that the present invention is applicable in many different environments. It is respectfully submitted that the cited reference fails to disclose or suggest all the elements of any of the presently pending claims. Therefore, the cited reference fails to provide the critical and unobvious advantages discussed above.

Goodrum relates to a method and apparatus for identifying faulty devices in a computer system. *Goodrum* describes detecting for a faulty condition associated with devices and identifying the device causing the faulty condition. The faulty condition includes a bus hang condition. The devices are turned off when a bus hang condition is detected. The devices are turned back on to test the devices. Information on the bus associated with the faulty condition is stored. The stored information is retrieved after the faulty condition has occurred. The stored information includes address, data and bus control information. Referring to Figure 38 of *Goodrum*, a BIOS automatic server recovery handler is invoked in response to an automatic server recovery reboot condition.

The automatic server recovery handler first checks to determine if an isolation-in progress event variable (EV) contains active information indicating that the isolation process was in progress prior to the automatic server recovery time-out event. The isolation-in progress EV is stored in non-volatile memory 70 and includes header information that is set active to indicate that the isolation process has started. *Goodrum*, however, does not disclose or suggest the feature of an interface circuit provided with a first register and a second register, wherein the bus address is transferred into the first register and the bus address is transferred, in conjunction with a reboot, from the first register into the second register.

In contrast, claim 6 recites a first register and a second register, and "means for transferring a bus address into the first register and means for transferring the bus address, in conjunction with a reboot, from the first register into the second register." Applicants respectfully submit that the cited reference does not disclose or suggest at least these features of the presently pending claims. Applicants respectfully traverse and submit that claims 6 and 7 are not anticipated by *Goodrum*.

Applicants submit that the in-progress event variable (EV) does not disclose or suggest first and second registers that are used in maintenance operations. According to *Goodrum*, the EV includes information regarding isolation processes and is stored in a non-volatile memory. This aspect of *Goodrum* does not disclose or suggest means for transferring a bus address into the first register. Thus, the information stored according to *Goodrum* does not disclose or suggest the bus address transferred into the first register

and transferred, in conjunction with a reboot, from the first register into the second register.

Applicants also submit that the non-volatile memory for storing isolation-in-progress EV does not disclose or suggest a first and second register. *Goodrum* describes the isolation-in-progress EV including header information that is set active to indicate that the isolation process has started. Applicants submit that this feature of isolation-in-progress EV does not disclose or suggest means for transferring a bus address, as recited in claim 6. Thus, *Goodrum* does not disclose or suggest all the features of claim 6. Claim 7 depends from claim 6, and is not disclosed or suggested by *Goodrum*, at least for the reasons given above. Applicants respectfully request that the anticipation rejection be withdrawn.

Claims 1, 2 and 4 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Goodrum* in further view of U.S. Patent No. 5,878,237 (*Olarig*). The Office Action took the position that *Goodrum* does not disclose "that the first plug-in unit addresses the second plug-in unit with the bus address, device-to-device transactions." The Office Action then took the position that *Olarig* taught those features of the claims missing from *Goodrum*. Applicants respectfully traverse, and submit that the cited references, either alone or in combination, do not disclose or suggest all the features of any of the presently pending claims.

Claim 1, upon which claims 2 and 3 are dependent, presently recites a method for identifying a defective plug-in unit in a system. The system includes a first bus, an

interface circuit provided with a first register and a second register, at least two plug-in units connected via interface circuits to the first bus, a second bus connected to at least one plug-in unit, and an operation and maintenance facility connected to the second bus. In the method, a first plug-in unit of the at least two plug-in units addresses a second plug-in unit of the at least two plug-in units with a bus address. The bus address is transferred into the first register. The bus address is transferred, in conjunction with a reboot, from the first register into the second register.

Claim 4, upon which claim 5 is dependent, presently recites a system for identifying a defective plug-in unit. The system includes a first bus. The system also includes an interface circuit provided with a first register and a second register. The system also includes at least two plug-in units connected via interface circuits to the first bus, a first plug-in unit comprising means for addressing a second plug-in unit with a bus address. The system also includes a second bus connected to at least one plug-in unit. The system also includes an operation and maintenance facility connected to the second bus. The system also includes means for transferring the bus address into the first register. The system also includes means for transferring the bus address, in conjunction with a reboot, from the first register into the second register. The system also includes means for reading the bus address from the second register by using an operation and maintenance facility.

Goodrum is summarized above with regard to claims 6-7. Applicants submit that *Goodrum* does not disclose or suggest all the features of claims 1, 2 and 4. As discussed

above, *Goodrum* does not disclose or suggest an interface circuit provided with a first register and a second register, wherein the bus address is transferred into the first register and the bus address is transferred, in conjunction with a reboot, from the first register into the second register. Applicants further submit that *Olarig* does not disclose or suggest these features of the claims missing from *Goodrum*.

Olarig relates to an apparatus, method and system for a computer CPU and memory to a PCI bridge having a plurality of physical PCI busses. *Olarig* describes a chip set in a computer system providing a bridge between processor host and memory busses, and a plurality of peripheral component interconnect (PCI) busses capable of operating at 66 MHz. The chip set has an arbiter having Request and Grant signal lines for each PCI device connected to the plurality of PCI physical busses. Upper and lower memory address range registers store upper and lower memory addresses associated with each PCI device. Whenever a transaction occurs, the transaction address is compared with the stored range of memory addresses. If a match between addresses is found then strong ordering is used. If no match is found, then weak ordering may be used to improve transactional latency times. *Olarig*, however, does not disclose or suggest an interface circuit provided with a first register and a second register, wherein the bus address is transferred into the first register and the bus address is transferred, in conjunction with a reboot, from the first register into the second register.

In contrast, claim 1 recites "an interface circuit provided with a first register and a second register, wherein the bus address is transferred into the first register and the bus

address is transferred, in conjunction with a reboot, from the first register into the second register." Applicants submit that the cited references, either alone or in combination, do not disclose or suggest at least these features of the presently pending claims.

Olarig describes upper and lower memory address range registers storing upper and lower memory addresses associated with PCI devices. This aspect of *Olarig* does not disclose or suggest transferring a bus address into a first register and then transferring the bus address, in conjunction with a reboot, from the first register into the second register. *Olarig* does not disclose or suggest transferring bus addresses between the upper and lower memory address range registers, as recited in the claims. Further, *Olarig* does not disclose or suggest detecting a fault situation and performing recovery operations following a reboot. Thus, *Olarig* does not disclose or suggest those features of the pending claims missing from *Goodrum*. Applicants respectfully request that the obviousness rejection of claims 1, 2 and 4 be withdrawn.

Claims 3, 5, and 8 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Goodrum*, in view of the CompactPCI Short Form Specification. The Office Action took the position that *Goodrum* does not teach "the first bus is a CompactPCI bus." The Office Action then took the position that CompactPCI Short Form Specification teaches those features of claims 3 and 5 missing from *Goodrum*. Applicants respectfully traverse, and submit that the cited references, either alone or in combination, do not disclose or suggest all the features of any of the presently pending claims.

Claim 3 is dependent upon claim 1. Claim 1 is summarized above.

Claim 5 is dependent upon claim 4. Claim 4 is summarized above.

Claim 8 is dependent upon claim 6. Claim 6 is summarized above.

CompactPCI Short Form Specification (CSFS) relates to an adaptation of the Peripheral Component Interconnect Specification for industrial and/or embedded applications requiring more robust mechanical form factor from desktop PCI. CompactPCI uses industry standard mechanical components and high-performance connector technologies to provide a system optimized for rugged applications. CompactPCI adaptor boards provide a front plate interface that is consistent with eurocard packaging. A CompactPCI system may be composed of up to 8 CompactPCI card locations. A system slot provides arbitration, clock distribution, and reset functions for all adaptors on the bus. CSFS, however, does not disclose or suggest the feature of an interface circuit provided with a first register and a second register, wherein the bus address is transferred into the first register and the bus address is transferred, in conjunction with a reboot, from the first register into the second register.

In contrast, as noted above, claim 1 recites "an interface circuit provided with a first register and a second register, wherein the bus address is transferred into the first register and the bus address is transferred, in conjunction with a reboot from the first register into the second register." Claim 4 recites "an interface circuit provided with a first register and a second register" and "means for transferring the bus address into the first register, means for transferring the bus address, in conjunction with a reboot, from

the first register into the second register, and means for reading the bus address from the second register by using the operation and maintenance facility." Claim 6 recites similar features as claims 1 and 4, but is drawn to an interface circuit. Applicants submit that the cited references, either alone or in combination, do not disclose or suggest at least these features of the presently pending claims.

The specification outlined by the CSFS does not disclose or suggest a first and a second register having bus addresses transferred to them. Further, the CSFS does not disclose or suggest means for transferring the bus address, in conjunction with a reboot, from the first register to the second register. Applicants submit that the CSFS does not disclose or suggest at least these features of the pending claims missing from *Goodrum*.

Further, claims 3, 5, and 8 are dependent either directly or indirectly from independent claims 1, 4, and 6, respectively. The independent claims are not rendered obvious by the cited references. If an independent claim is not obvious, then any claim depending therefrom also is not obvious. MPEP 2143.03. Thus, claims 3, 5, and 8 are not rendered obvious by the cited references, either alone or in combination. Further, claims 3, 5, and 8 recite subject matter in addition to the independent claims that also is not disclosed or suggested by the cited references. Applicants respectfully request that the obviousness rejection of claims 3, 5, and 8 be withdrawn.

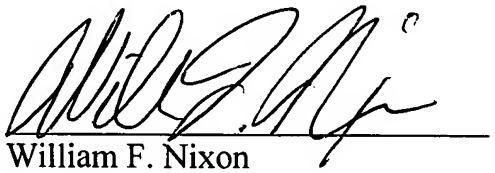
It is submitted that each of claims 1-8 recites subject matter that is neither disclosed nor suggested by the cited references, either alone or in combination. It is

therefore respectfully requested that all of claims 1-8 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



William F. Nixon
Registration No. 44,262

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

WFN:cct